Attorney's Docket No.: 10559-596001/P12880

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : William R. Wheeler et al. Art Unit: 2812
Serial No.: 09/941,158 Examiner:
Filed : August 28, 2001 Stacy Whitmore
Assignee : Intel Corporation
Title : MODEL-BASED LOGIC DESIGN

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicants call attention to the attached Information Disclosure Statement and documents listed on form PTO-1449.

Copies of the U.S. patents and publications are not being provided per the waiver posted on the PTO website.

This filing is being made before the receipt of a first Office action on the merits. No fee is required.

The documents are in the English language; hence no concise explanation is necessary per Rule 98(a)(3).

Consideration of the foregoing and enclosures plus the return of a copy of the enclosed form PTO-1449 with the

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

April 29, 2004
Date of Deposit

Signature

Jennifer H. Payne
Typed or Printed Name of Person Signing Certificate

Examiner's initials in the left column per MPEP 609 are earnestly solicited along with an early action on the merits.

Please apply any additional charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 4/29/04

Scott C. Harris
Reg. No. 32,030
Attorney for Intel Corporation

Fish & Richardson P.C.
USPTO Customer No. **20985**
12390 El Camino Real
San Diego, CA 92130
Telephone: (858) 678-5070
Facsimile: (858) 678-5099

10390743.doc

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-596001	Application No. 09/941,158
Information Disclosure Statement by Applicant (Use several sheets if necessary)		Applicant William R. Wheeler et al.	
(37 CFR §1.98(b))		Filing Date August 28, 2001	Group Art Unit 2812

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	RE 38,059	04/2003	Yano, et al.			
	AB	4,703,435	10/1987	Darringer, et al.			
	AC	4,970,664	11/1990	Kaiser, et al.			
	AD	5,212,650	05/1993	Hooper, et al.			
	AE	5,267,175	11/1993	Hooper			
	AF	5,278,769	01/1994	Bair, et al.			
	AG	5,287,289	02/1994	Kageyama, et al.			
	AH	5,297,053	03/1994	Pease, et al.			
	AI	5,301,318	04/1994	Mittal			
	AJ	5,384,710	01/1995	Lam, et al.			
	AK	5,475,605	12/1995	Lin			
	AL	5,493,507	02/1996	Shinde, et al.			
	AM	5,544,067	08/1996	Rostoker, et al.			
	AN	5,568,397	10/1996	Yamashita, et al.			
	AO	5,598,347	01/1997	Iwasaki			
	AP	5,603,015	02/1997	Kurosawa, et al.			
	AQ	5,604,894	02/1997	Pickens, et al.			
	AR	5,663,662	09/1997	Kurosawa			
	AS	5,673,198	09/1997	Lawman, et al.			
	AT	5,685,006	11/1997	Shiraishi			
	AU	5,694,579	12/1997	Razdan, et al.			
	AV	5,706,476	01/1998	Giramma			
	AW	5,717,928	02/1998	Campmas, et al.			
	AX	5,724,250	03/1998	Kerzman, et al.			
	AY	5,757,655	05/1998	Shih, et al.			
	AZ	5,809,283	09/1998	Vaidyanathan, et al.			
	AAA	5,831,869	11/1998	Ellis, et al.			

Examiner Signature	Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-596001	Application No. 09/941,158
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant William R. Wheeler et al.	
		Filing Date August 28, 2001	Group Art Unit 2812

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	ABB	5,841,663	11/1998	Sharma, et al.			
	ACC	5,892,682	04/1999	Hasley, et al.			
	ADD	5,903,469	05/1999	Ho			
	AEE	5,937,190	08/1999	Gregory, et al.			
	AFF	5,974,242	10/1999	Damarla, et al.			
	AGG	6,077,304	06/2000	Kasuya			
	AHH	6,161,211	12/2000	Southgate			
	AII	6,178,541	01/2001	Joly, et al.			
	AJJ	6,208,954	03/2001	Houtchens			
	AKK	6,216,256	04/2001	Inoue, et al.			
	ALL	6,226,780	05/2001	Bahra, et al.			
	AMM	6,234,658	05/2001	Houldsworth			
	ANN	6,275,973	08/2001	Wein			
	AOO	6,292,931	09/2001	Dupenloup			
	APP	6,327,693	12/2001	Cheng, et al.			
	AQQ	6,353,806	03/2002	Gehlot			
	ARR	6,353,915	03/2002	Deal, et al.			
	ASS	6,360,356	03/2002	Eng			
	ATT	6,381,563	04/2002	O'Riordan, et al.			
	AUU	6,381,565	04/2002	Nakamura			
	AVV	6,421,816	07/2002	Ishikura			
	AWW	6,438,729	08/2002	Ho			
	AXX	6,438,731	08/2002	Segal			
	AYY	6,440,780	08/2002	Kimura, et al.			
	AZZ	6,473,885	10/2002	Wallace			
	AAAA	6,477,688	11/2002	Wallace			
	ABBB	6,490,545	12/2002	Peng			

Examiner Signature	Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-596001	Application No. 09/941,158
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant: William R. Wheeler et al.	
		Filing Date: August 28, 2001	Group Art Unit: 2812

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	ACCC	6,505,328	01/2003	Van Ginneken, et al.			
	ADDD	6,516,456	02/2003	Garnett, et al.			
	AEEE	6,519,742	02/2003	Falk			
	AFFF	6,523,156	02/2003	Cirit			
	AGGG	6,539,536	03/2003	Singh et al.			
	AHHH	6,546,528	04/2003	Sasaki, et al.			
	AIII	6,574,787	06/2003	Anderson			
	AJJJ	6,591,407	07/2003	Kaufman, et al.			
	AKKK	2002/0112221	08/2002	Ferreri, et al.			
	ALLL	2002/0138244	09/2002	Meyer			
	AMMM	2003/0004699	01/2003	Choi, et al.			
	ANNN	2003/0036871	02/2003	Fuller, et al.			
	AOOO	2003/0177455	09/2003	Kaufman, et al.			

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	APPP	0 404 482	12/1990	EPO				
	AQQQ	0 720 233	07/1996	EPO				
	ARRR	0 901 088	03/1999	EPO				
	ASSS	58-060559	04/1983	Japan				
	ATTT	03-225523	10/1991	Japan				
	AUUU	07-049890	02/1995	Japan				
	AVVV	08-314892	11/1996	Japan				
	AWWW	2001-068994	03/2001	Japan				
	AXXX	WO 98/37475	08/1998	WIPO				
	AYYY	WO 98/55879	12/1998	WIPO				
	AZZZ	WO 99/39268	08/1999	WIPO				

Examiner Signature	Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-596001	Application No. 09/941,158
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant William R. Wheeler et al.	
		Filing Date August 28, 2001	Group Art Unit 2812

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	AAAAA	Gassenfeit, E. H., "Control System Design Realization via VHDL-A: Requirements", Proceedings of the 1996 IEEE International Symposium on Computer-Aided Control System Design, September 15, 1996, pp. 282-285.
	ABBBB	Kutzschebauch, "Efficient logic optimization using regularity extraction", Proceedings of 2000 International Conference on Computer Design, September 17, 2000, pp. 487-493.
	ACCCC	Lahti, et al., "SADE: a Graphical Toll for VHDL-Based System Analysis", 1991 IEEE International Conference on Computer-Aided Design, November 11, 1991, pp. 262-265.
	ADDDD	Lin, et al., "A Goal Tree Based High-Level Test Planning System for DSP Real Number Models", 1998 Proceedings of International Test Conference, October 18, 1998, pp. 1000-1009.
	AEEEE	Maxfield, C., "Digital Logic Simulation: Event-Driven, Cycle-Based, and Home-Brewed", *Electrical Design News*, 41(14):129-136 (1996).
	AFFFF	NB84035598, "Binary Relational Schema to Model Structured LSI Design", IBM Technical Disclosure Bulletin, Vol. 26, No. 10B, March 1984, pp. 5598-5601.
	AGGGG	NN7807629, "Functional Oriented Symbolic Macromodeling Algorithm", IBM Technical Disclosure Bulletin, Vol. 21, No. 2, July 1978, pp. 629-631.
	AHHHH	NN8006341, "Macro Physical-To-Logical Checking LSI Chip Design", IBM Technical Disclosure Bulletin, Vol. 23, No. 1, June 1980, pp. 341-345.
	AIIII	NN9407481, "Functional Modeling using object Collaboration Diagram", IBM Technical Disclosure Bulletin, Vol. 37, No. 7, July 1994, pp. 481-486.
	AJJJJ	Parlakbilek, et al., "A Multiple-Strength Multiple-Delay Compiled-Code Logic Simulator", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 12(12):1937-1946 (1993).
	AKKKK	Su, Stephen, "An Interactive Design Automation System", *Proceedings of the 10th Design Automation Workshop on Design Automation*, pp. 253-261, June 1973
	ALLLL	Yli-Pietila, et al., "The Design and Simulation of Complex Multitechnology Systems", IEEE International Conference on Systems Engineering, August 9, 1990, pp. 474-477.

Examiner Signature	Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.